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High Speed Max-Log-MAP Turbo SISO Decoder Implementation

...

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Use Verilog HDL building blocks (design units) including modules, ports, processes, and assignments Model code styles including behavioral code style and structural code style Understand the design methodologies of Verilog HDL and the differences between simulation models and synthesis models

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Verilog HDL Basics - Intel

The converter analyzes the code of each generator and maps it to equivalent constructs in the target HDL. For Verilog, it will map generators to always blocks, continuous assignments or initial blocks. For VHDL, it will map them to process statements or concurrent signal assignments. The module ports are inferred from signal usage

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7.4.1. Combinational design in asynchronous circuit]. Fig. 7.4 shows the truth-table for (2×1) multiplexer and corresponding Karnaugh map is shown in Fig. 7.5. Note that, the glitches occurs in the circuit, when we exclude the red part of the solution from the Fig. 7.5, which results in minimum-gate solution,

but at the same time the solution is disjoint.

Verilog Code for Ripple Carry Adder - FPGA4student.com
Karnaugh-map for 2 , 3 and 4 variables in both sum of product and product of sum expressions, which takes min-terms or max-terms as input and return simplified expression with desired variables.
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Parameters are Verilog constructs that allow a module to be reused with a different specification. For example, a 4-bit adder can be parameterized to accept a value for the number of bits and new parameter values can be passed in during module instantiation. So, an N-bit adder can become a 4-bit, 8-bit or 16-bit adder.

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This contains BER simulation both Log-MAP and Max-Log MAP for a range of E_b/N_0 with graphical representation of BER Vs E_b/N_0 . For any clarifications on this code, Reach me through comment box. Cite As Vinay kumar Reddy (2020).

7. Finite state machine □ FPGA designs with Verilog and ...

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Verilog Parameters - ChipVerify

Flappy Bird on FPGA Spartan 3 Verilog code. Contribute to themaxaboy/Flappy-Bird-Verilog development by creating an account on GitHub.

Edit code - EDA Playground

The authors present a turbo soft-in soft-out (SISO) decoder based on Max-Log maximum a posteriori (ML-MAP) algorithm implemented with sliding window (SW) method. A novel technique based on branch metric normalization is introduced to improve the speed performance of the decoder. The turbo decoder with the proposed technique has been synthesized to evaluate its power consumption and area usage ...

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