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Virtex-5 FPGA slices are organized differently from previous generations. Each Virtex -5 FPGA slice contains four LUTs and four flip-flops (previously it was two LUTs and two flip-flops.) 2. Each DSP48E slice contains a 25 x 18 multiplier, an adder, and an accumulator. 3. Block RAMs are fundamentally 36 Kbits in size.

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User Guide: Please refer to this user manual, keeping in mind that the XUPV5-LX110T development system hosts a Virtex 5 LX 110T device. All other user interfaces remain the same. Xilinx ML505 User Manual

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